INTERSIL
SYSTEMS DIVISION

ISB-3100 Z80 Central Processor Card

FEATURES

- Full STD BUS Compatibility
- Fully Buffered Signals for System Expandability
- Up to 8K Bytes EPROM Capacity
- Up to 4K Bytes Static RAM Capacity
- Jumper Selectable (2716 or 2732 EPROMs)
- Full Memory Decoding Capability
- Full Bus Arbitration Circuitry
- Four Independent Timer/Counter Channels
- Programmable Power-on Restart
- 4 MHz Clock Frequency
- Internal/External Clock Selection
- Tri-state Address, Data and Control Bus
- Single +5V Supply
- Optional One Wait State During Any Memory Cycle

GENERAL DESCRIPTION

The ISB-3100 is a Z80A based STD BUS microprocessor card with a 250ns clock time. The entire Z80A-CPU Instruction Set can be used for programming without restriction. All signals to and from the STD BUS (address, data, and control) are fully tri-state buffered. Bus arbitration logic ensures proper arbitration between on-board vs off-board memory, I/O, or interrupt acknowledge operations.

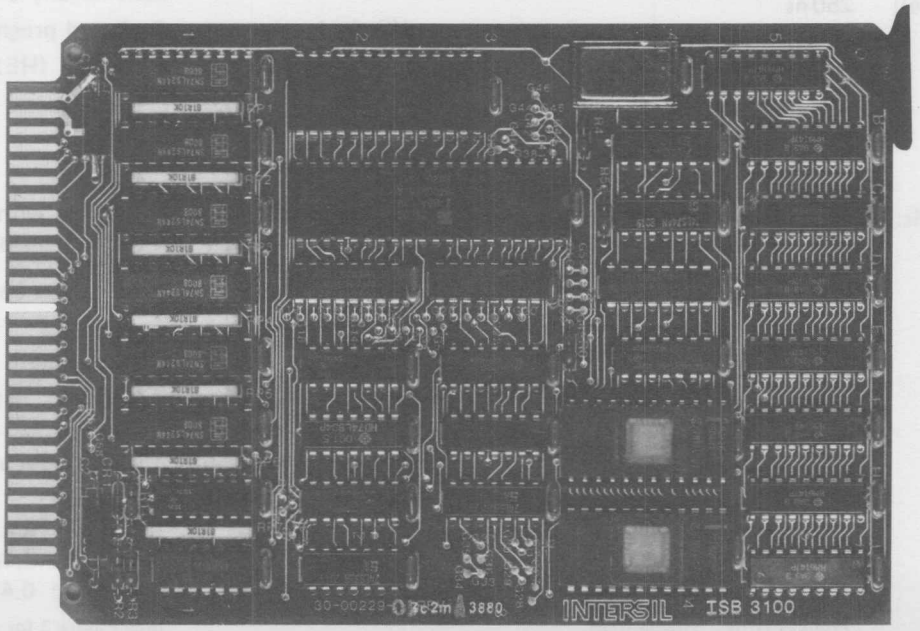
On-board static RAM memory in 1K Byte increments up to a maximum of 4K are provided. The popular 2114 (1K x 4) static RAM with 200ns access time is used. Two 24-pin sockets are provided for EPROM memory. Up to 4K Bytes of EPROM memory are available using 2716's (2K x 8) or up to 8K using 2732's (4K x 8).

Memory mapping for on-board RAMs and EPROMs is jumper selectable and can be mapped in 4K blocks anywhere in the 64K address field in 4K increments. The on-board RAMs and EPROMs can also be totally bypassed and removed from the card. One wait state is inserted during any memory operation. This circuitry can also be disabled so there is no wait state.

An on-board Counter Timer Circuit (CTC) provides four independent channels that provide counting and timing functions with interrupting capability and daisy chain priority arbitration.

Both on-board power-on reset and off-board pushbutton reset are implemented. The CPU on reset will start at 0000_H or can be programmed to jump to any location within the address field. If the latter is chosen, 3 bytes of the first EPROM on the board are used to store the jump address. After reading the starting address, the circuitry disables the EPROM or maps it at other preassigned locations other than 0000_H.

Jumper options include: CPU clock (internal/external), CTC clock by channel (internal/external), on-board RAM starting address (anywhere in the 64K address field in 4K increments), on-board EPROM starting address (anywhere in the 64K address field in 4K increments), reset restart address (anywhere within on-board memory address range), EPROM type selection (2716 or 2732), wait state (enabled/disabled).



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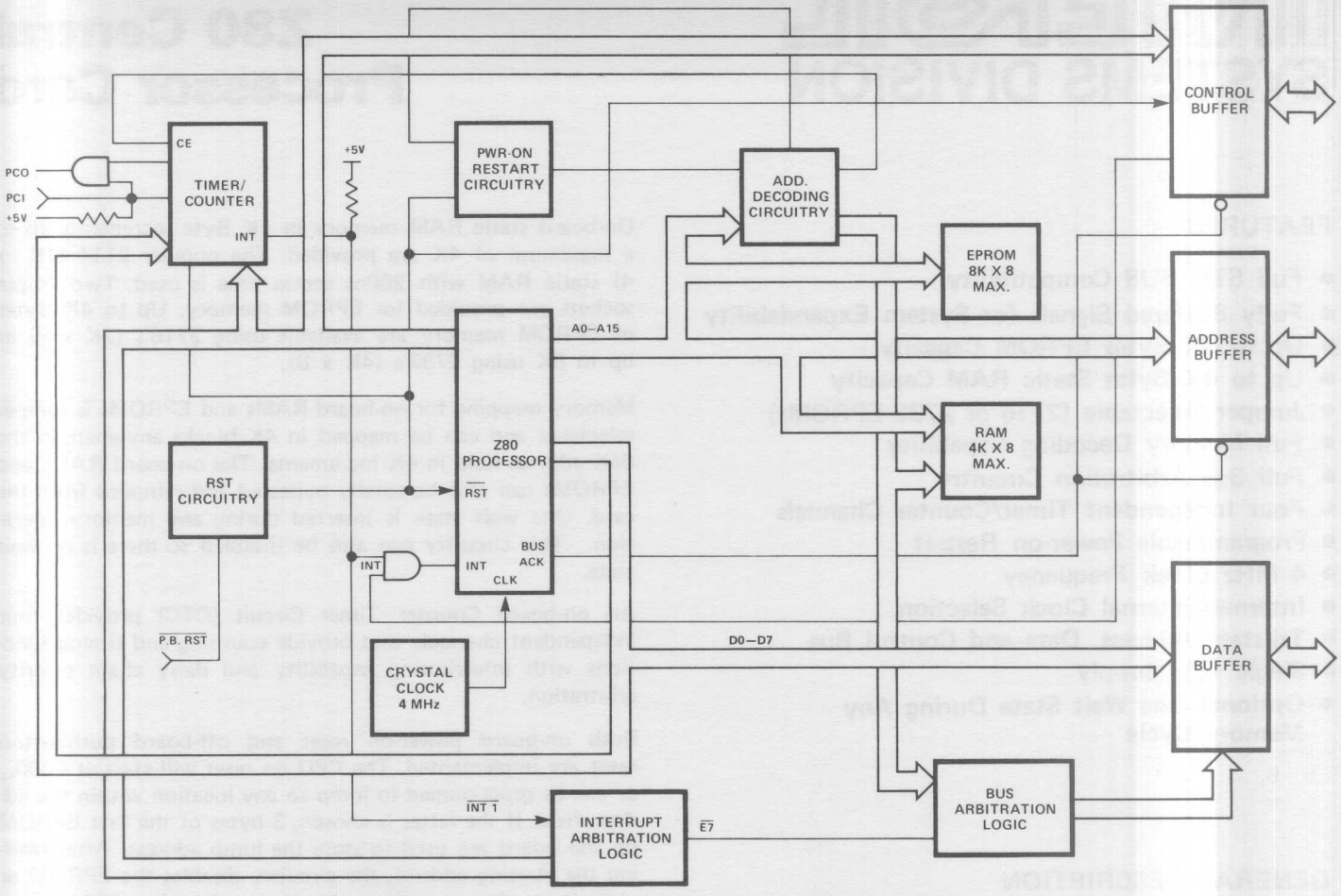

FIGURE 1. ISB-3100 Block Diagram

SPECIFICATIONS

Word Size:	8 Bit Data Bus Instruction: 8, 16, 24, 32 bits
Clock Period (T state):	250 ns
Memory Capacity:	On-board EPROMs—Up to 8K Bytes On-board RAMs—Up to 4K Bytes Off-board Expansion—Up to 64K Bytes with customer specified combination of RAMs, ROMs, EPROMs
Memory Mapping:	
On-board EPROMs:	Jumper selectable 2716 (2K bytes) or 2732 (4K bytes) Jumper selectable for any 4K boundary within 64K address field. If 2732 is used, two 4K EPROMs can be mapped independently from each other within a 64K address field.
On-board RAMs:	Jumper selectable for any 4K boundary within a 64K address field.
Memory Speed:	EPROM: 2716 or 2732 Access time: 450ns max. RAM: Dynamic or static Access time: 450ns max.
I/O Capacity:	Up to 256 Bytes can be decoded off-board. The four port addresses, (7C, 7D, 7E, 7F) are used for on-board timer/counter and cannot be used for any off-board peripherals.
I/O Addressing:	On-board programmable timer

Port Addr (HEX)	CTC Chan.
7C	0
7D	1
7E	2
7F	3

Interrupts:	Multi-level with three vectoring modes. Interrupt request may originate from customer specified I/O or from the on-board CTC.
System Clock:	4 MHz max. 500 kHz min.
Interface:	All address, data and command signals are TTL compatible.
Power Requirement:	+5 VDC ±5% at 1.5 amps max.
Mating Connectors:	See Table 1
Card Dimension:	Height: 6.5 inches (16.51 cm) Width: 4.48 inches (11.38 cm) Thickness: 0.44 inches (1.12 cm) (See Figure 3 for more details)

ENVIRONMENTAL REQUIREMENTS

Operating Temperature: 0° to 55°C
Storage Temperature: −40° to 80°C
Relative Humidity: 0% to 90% without condensation

TABLE 1. ISB-3100 Compatible Mating Connectors

INTERFACE	NO. OF PAIRS/PINS	CENTERS	CONNECTOR TYPE	VENDOR	VENDOR PART NO.
STD BUS	28/56	0.125 in.	Solder Tail	Viking Winchester	VH28/ICNK5 2HW28 D0−111
STD BUS	28/56	0.125 in.	Wire Wrap	Viking Winchester	VH28/ICHD5 HW28 D0−111

TABLE 2. ISB-3100 STD BUS Organization and Functional Specifications (With Pin Definitions)

The STD BUS pinout is organized into five functional groups:

Logic Power Bus	Pins 1−6
Data Bus	Pins 7−14
Address Bus	Pins 15−30
Control Bus	Pins 31−52
Auxiliary Power Bus	Pins 53−56

COMPONENT SIDE				CIRCUIT SIDE			
PIN	MNEMONIC	SIGNAL FLOW	DESCRIPTION	PIN	MNEMONIC	SIGNAL FLOW	DESCRIPTION
1	+5V	In	+5 Volts DC (Bussed)	2	+5V	In	+5 Volts DC (Bussed)
3	GND	In	Digital Ground (Bussed)	4	GND	In	Digital Ground (Bussed)
5	−5V	In	−5 Volts DC	6	−5V	In	−5 Volts DC
7	D3	In/Out	Low Order Data Bus	8	D7	In/Out	High Order Data Bus
9	D2	In/Out	Low Order Data Bus	10	D6	In/Out	High Order Data Bus
11	D1	In/Out	Low Order Data Bus	12	D5	In/Out	High Order Data Bus
13	D0	In/Out	Low Order Data Bus	14	D4	In/Out	High Order Data Bus
15	A7	Out	Low Order Address Bus	16	A15	Out	High Order Address Bus
17	A6	Out	Low Order Address Bus	18	A14	Out	High Order Address Bus
19	A5	Out	Low Order Address Bus	20	A13	Out	High Order Address Bus
21	A4	Out	Low Order Address Bus	22	A12	Out	High Order Address Bus
23	A3	Out	Low Order Address Bus	24	A11	Out	High Order Address Bus
25	A2	Out	Low Order Address Bus	26	A10	Out	High Order Address Bus
27	A1	Out	Low Order Address Bus	28	A9	Out	High Order Address Bus
29	A0	Out	Low Order Address Bus	30	A8	Out	High Order Address Bus
31	$\overline{WR}$	Out	Write to Memory or I/O	32	$\overline{RD}$	Out	Read to Memory or I/O
33	$\overline{IORQ}$	Out	I/O Address Select	34	$\overline{MEMRQ}$	Out	Memory Address Select
35	$\overline{IOEXP}$	In/Out	I/O Expansion	36	$\overline{MEMEX}$	In/Out	Memory Expansion
37	$\overline{REFRESH}$	Out	Refresh Timing	38	$\overline{MCSYNC}$	Out	CPU Machine Cycle Sync
39	$\overline{STATUS\ 1}$	Out	CPU Status	40	$\overline{STATUS\ 0}$	Out	CPU Status
41	$\overline{BUSAK}$	Out	Bus Acknowledge	42	$\overline{BUSRQ}$	In	Bus Request
43	$\overline{INTAK}$	Out	Interrupt Acknowledge	44	$\overline{INTRQ}$	In	Interrupt Request
45	$\overline{WAITRQ}$	In	Wait Request	46	$\overline{NMIRQ}$	In	Non-Maskable Interrupt
47	$\overline{SYSRESET}$	Out	System Reset	48	$\overline{PBRESET}$	In	Push Button Reset
49	$\overline{CLOCK}$	Out	Clock from Processor	50	$\overline{CNTRL}$	In	AUX Timing
51	PCO	Out	Priority Chain Out	52	PCI	In	Priority Chain In
53	AUX GND	In	AUX Ground (Bussed)	54	AUX GND	In	AUX Ground (Bussed)
55	AUX+V	In	AUX Positive (+12 Volts DC)	56	AUX−V	In	AUX Negative (−12 Volts DC)

TABLE 3. ISB-3100 STD BUS Signal Functions

SIGNAL	PIN NO.	FUNCTIONAL DESCRIPTION
+5V	1 & 2	*+5 Logic Voltage (V_{CC})* – Main logic voltage lines (+5 volts). Both pins are bussed together for current capacity.
GND	3 & 4	*Logic Ground* – Ground for logic power. Both pins are bussed together for current capacity.
–5V	5 & 6	*–5 Logic Voltage* – Both pins are bussed together for current capacity.
D0–D7	7–14	*Data Bus* – An 8-Bit bidirectional tri-state bus. (Bidirectional means signals may flow either into or out of any card on the Bus). Direction of data is normally controlled by the processor card via the Control Bus. The data direction is normally affected by such signals as Read ($\overline{RD}$), Write ($\overline{WR}$) and Interrupt Acknowledge ($\overline{INTAK}$). The Data Bus uses high-level active logic levels. All cards are required to release the bus to a high impedance state when not in use. The Processor card releases the data bus in response to Bus Request ($\overline{BUSRQ}$) input from an alternate system controller, as in DMA transfers.
A0–A15	15–30	*Address Bus* – A 16-bit tri-state high-level active bus. The address will originate at the processor card or a bus controlling device. The processor card releases the Address Bus in response to a Bus Request ($\overline{BUSRQ}$) input from an alternate controller. The Address Bus provides 16 address lines for decoding by either memory or I/O. Memory request ($\overline{MEMRQ}$) and I/O request ($\overline{IORQ}$) control lines are used to distinguish between the two operations.
$\overline{WR}$	31	*Write to Memory or I/O* – A tri-state, active-low control line that indicates the BUS holds valid data to be written in the addressed memory or output device.
$\overline{RD}$	32	*Read from Memory or I/O* – A tri-state, active-low control line that indicates the processor or other bus controlling device wants to read data from memory or an I/O device. The selected I/O device or memory should use this signal to gate data onto the BUS.
$\overline{IORQ}$	33	*I/O Address Select* – A tri-state, active-low processor output control line. $\overline{IORQ}$ indicates that the address lines hold a valid I/O address for an I/O Read or Write.
$\overline{MEMRQ}$	34	*Memory Address Select* – A tri-state, active-low memory request line. $\overline{MEMRQ}$ indicates that the Address Bus holds a valid address for memory read or memory write operations.
$\overline{IOEXP}$	35	*I/O Expansion* – An active-low control signal used to expand or enable I/O Port addressing.
$\overline{MEMEX}$	36	*Memory Expansion* – An active-low control signal used to expand or enable memory addressing.
$\overline{REFRESH}$	37	*Dynamic Memory Refresh* – a tri-state, active-low control line normally used to refresh dynamic memory. This signal is generated on the processor card.
$\overline{MCSYNC}$	38	*Machine Cycle Sync* – A tri-state, active-low processor output signal that occurs once during each processor machine cycle. (Machine cycle is defined as the sequence that involves Addressing, Data Transfer and Execution.) $\overline{MCSYNC}$ defines the beginning of the machine cycle.
$\overline{STATUS\ 1}$	39	*Status Control Line 1* – $\overline{STATUS\ 1}$ is a signal to identify Instruction Fetch.

TABLE 3. ISB-3100 STD BUS Signal Functions (Continued)

SIGNAL	PIN NO.	FUNCTIONAL DESCRIPTION
$\overline{\text{STATUS 0}}$	40	*Status Control Line 0* – Status Control lines provide timing information related to special cycle operations. (Not used on the ISB-3100.)
$\overline{\text{BUSAK}}$	41	*BUS Acknowledge* – An active-low output line. The processor responds to a $\overline{\text{BUSRQ}}$ by releasing the BUS and giving an Acknowledge signal on the $\overline{\text{BUSAK}}$ line. $\overline{\text{BUSAK}}$ occurs at the completion of the current machine cycle.
$\overline{\text{BUSRQ}}$	42	*Bus Request* – An active-low input line. A $\overline{\text{BUSRQ}}$ causes the processor to suspend operations on the BUS by releasing all tri-state BUS lines for use by another processor. The BUS is released once the current machine cycle is completed.
$\overline{\text{INTAK}}$	43	*Interrupt Acknowledge* – An active-low output line from the processor card that occurs in response to ($\overline{\text{INTRQ}}$). It is used to tell the interrupting device that the processor card is ready to respond to the Interrupt. For vectored interrupts the vector address is placed on the Data Bus by the interrupting device during $\overline{\text{INTAK}}$.
$\overline{\text{INTRQ}}$	44	*Interrupt Request* – An active-low processor card input line that conditionally interrupts the program. It is masked and ignored by the processor unless deliberately enabled by a program instruction. If the processor accepts the interrupt, it acknowledges by dropping $\overline{\text{INTAK}}$.
$\overline{\text{WAITRQ}}$	45	*Wait Request* – An active-low input line to the processor that suspends processor operations as long as it remains low. The processor will hold in a state that maintains a Valid Address on the Address Bus.
$\overline{\text{NMIRQ}}$	46	*Non-Maskable Interrupt* – An active-low processor card interrupt input line of highest priority.
$\overline{\text{SYSRESET}}$	47	*System Reset* – An active-low output from the system reset circuit. The system reset circuit is triggered by power-on detection or by the pushbutton reset. The system reset bus line should be applied to all cards on the BUS that have latch circuits requiring initialization.
$\overline{\text{PBRESET}}$	48	*Push Button Reset* – An active-low input line to the processor.
$\overline{\text{CLOCK}}$	49	*Clock From Processor* – A buffered processor clock signal used for system synchronization or as a general clock source.
$\overline{\text{CNTRL}}$	50	*Control* – An external clock input for special clock timing.
PCO	51	*Priority Chain Output (Output, active-high)* – This signal is sent to the PCI input of the next lower card in the priority chain. A card that needs priority should hold PCO low.
PCI	52	*Priority Chain In (Input, active-high)* – This signal is provided directly from the PCO of the next higher card in the priority chain. A high level on PCI gives priority to the card sensing the PCI input.
AUX GND	53 & 54	*Auxiliary Ground* – Ground for AUX Power. Both pins bussed together for current capacity.
AUX +V	55	*Auxiliary Positive Voltage (+12 Volts DC)*
AUX –V	56	*Auxiliary Negative Voltage (–12 Volts DC)*

TABLE 4. ISB-3100 AC Characteristics

T_A = 0°C to 35°C, V_{CC} = +5V ±5%, Unless Otherwise Noted

SIGNAL	SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITIONS
Φ (A)	t_c	Clock Period	0.25	[12]	μs	
	$t_{w(\Phi H)}$	Clock Pulse Width, Clock High	110		ns	
	$t_{w(\Phi L)}$	Clock Pulse Width, Clock Low	110	2000	ns	
	$t_{r,f}$	Clock Rise and Fall Time		30	ns	
A_{0-15}	$t_{D(AD)}$	Address Output Delay		110	ns	C_L = 50pF
	$t_{F(AD)}$	Delay to Float		90	ns	
	t_{acm}	Address Stable Prior to $\overline{MREQ}$ (Memory Cycle)	[1]		ns	
	t_{aci}	Address Stable Prior to $\overline{IORQ}$, $\overline{RD}$ or $\overline{WR}$ (I/O Cycle)	[2]		ns	
	t_{ca}	Address Stable From $\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$ or $\overline{MEMRQ}$	[3]		ns	Except T3, $\overline{ST1}$
	t_{caf}	Address Stable From $\overline{RD}$ or $\overline{WR}$ During Float	[4]		ns	
D_{0-7}	$t_{D(D)}$	Data Output Delay		150	ns	C_L = 50pF
	$t_{F(D)}$	Delay to Float During Write Cycle		90	ns	
	$t_{S\Phi(D)}$	Data Setup Time to Falling Edge of Clock During $\overline{ST1}$ Cycle	50		ns	
	$t_{S\Phi(D)}$	Data Setup Time to Rising Edge at Clock During M2 to M5	60		ns	
	t_{dcm}	Data Stable Prior to $\overline{WR}$ (Memory Cycle)	[5]		ns	
	t_{dci}	Data Stable Prior to $\overline{WR}$ (I/O Cycle)	[6]		ns	
	t_{cdf}	Data Stable From $\overline{WR}$	[7]		ns	
	t_H	Input Hold Time	0		ns	
$\overline{MEMRQ}$	$t_{DL\Phi(MR)}$	$\overline{MEMRQ}$ Delay From Rising Edge of Clock, $\overline{MEMRQ}$ Low	30	95	ns	C_L = 50pF
	$t_{DH\bar{\Phi}(MR)}$	$\overline{MEMRQ}$ Delay From Falling Edge of Clock, $\overline{MEMRQ}$ High		95	ns	
	$t_{DH\Phi(MR)}$	$\overline{MEMRQ}$ Delay From Rising Edge of Clock, $\overline{MEMRQ}$ High		95	ns	
	$t_{w(MRL)}$	Pulse Width $\overline{MEMRQ}$ Low	[8]		ns	
	$t_{W(MRH)}$	Pulse Width, $\overline{MEMRQ}$ High	[9]		ns	
$\overline{IORQ}$	$t_{DL\bar{\Phi}(IR)}$	$\overline{IORQ}$ Delay From Falling Edge of Clock, $\overline{IORQ}$ Low		75	ns	C_L = 50pF
	$t_{DL\Phi(IR)}$	$\overline{IORQ}$ Delay From Rising Edge of Clock, $\overline{IORQ}$ Low		85	ns	
	$t_{DH\bar{\Phi}(IR)}$	$\overline{IORQ}$ Delay From Falling Edge of Clock $\overline{IORQ}$ High		85	ns	
	$t_{DH\Phi(IR)}$	$\overline{IORQ}$ Delay From Rising Edge of Clock, $\overline{IORQ}$ High		85	ns	
$\overline{RD}$	$t_{DL\bar{\Phi}(RD)}$	$\overline{RD}$ Delay From Falling Edge of Clock $\overline{RD}$ Low		85	ns	C_L = 50pF
	$t_{DL\Phi(RD)}$	$\overline{RD}$ Delay From Rising Edge of Clock, $\overline{RD}$ Low		95	ns	
	$t_{DH\bar{\Phi}(RD)}$	$\overline{RD}$ Delay From Falling Edge of Clock, $\overline{RD}$ High		85	ns	
	$t_{DH\Phi(RD)}$	$\overline{RD}$ Delay From Rising Edge of Clock, $\overline{RD}$ High		85	ns	
$\overline{WR}$	$t_{DL\bar{\Phi}(WR)}$	$\overline{WR}$ Delay From Falling Edge of Clock, $\overline{WR}$ Low		65	ns	C_L = 50pF
	$t_{DL\Phi(WR)}$	$\overline{WR}$ Delay From Rising Edge of Clock, $\overline{WR}$ Low		80	ns	
	$t_{DH\phi(WR)}$	$\overline{WR}$ Delay From Rising Edge of Clock, $\overline{WR}$ High		80	ns	
	$t_{w(WRL)}$	Pulse Width, $\overline{WR}$ Low	[10]		ns	
$\overline{STATUS\ 1}$	$t_{DL(M1)}$	$\overline{ST1}$ Delay From Falling Edge of Clock, $\overline{ST1}$ Low		100	ns	C_L = 50pF
	$t_{DH(M1)}$	$\overline{ST1}$ Delay From Falling Edge of Clock, $\overline{ST1}$ High		100	ns	
$\overline{REFRESH}$	$t_{DL(RF)}$	Refresh Delay From Falling Edge of Clock, $\overline{REFRESH}$ Low		130	ns	C_L = 50pF
	$t_{DH(RF)}$	Refresh Delay From Falling Edge of Clock, $\overline{REFRESH}$ High		120	ns	
$\overline{WAIT}$	$t_{S(WT)}$	$\overline{WAIT}$ Setup Time to Rising Edge of Clock	70		ns	
$\overline{HALT}$	$t_{D(HT)}$	$\overline{HALT}$ Delay Time From Rising Edge of Clock		300	ns	C_L = 50pF
$\overline{INTRQ}$	$t_{s(IT)}$	$\overline{INTRQ}$ Setup Time to Falling Edge of Clock	80		ns	
$\overline{NMIRQ}$	$t_{w(\overline{NML})}$	Pulse Width, $\overline{NMIRQ}$ Low	80		ns	
$\overline{BUSRQ}$	$t_{s(BQ)}$	$\overline{BUSRQ}$ Setup Time to Falling Edge of Clock	50		ns	
$\overline{BUSAK}$	$t_{DL(BA)}$	$\overline{BUSAK}$ Delay From Falling Edge of Clock, $\overline{BUSAK}$ Low		100	ns	C_L = 50pF
	$t_{DH(BA)}$	$\overline{BUSAK}$ Delay From Rising Edge of Clock, $\overline{BUSAK}$ High		100	ns	
$\overline{RESET}$	$t_{s(RS)}$	$\overline{RESET}$ Setup Time to Falling Edge of Clock (C)	60		ns	
	$t_{F(C)}$	Delay To/From Float ($\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$ and $\overline{WR}$)		80	ns	
	t_{mr}	$\overline{STATUS1}$ Stable Prior to $\overline{IORQ}$ (Interrupt Ack.)	[11]		ns	

NOTE A. $\bar{\Phi}$ designates $\overline{CLOCK}$ on the STD BUS.

NOTE B. Data should be enabled onto the CPU data bus when $\overline{RD}$ is active. During interrupt acknowledge data should be enabled when $\overline{ST1}$ and $\overline{IORQ}$ are both active.

NOTE C. The $\overline{RESET}$ signal must be active for a minimum of 3 clock cycles.

[1] $t_{acm} = t_W\ (\Phi H) + t_f - 65$
[2] $t_{aci} = t_c - 70$
[3] $t_{ca} = t_W\ (\Phi L) + t_r - 50$
[4] $t_{caf} = t_W\ (\Phi L) + t_r - 45$
[5] $t_{dcm} = t_c - 170$
[6] $t_{dci} = t_W\ (\Phi L) + t_r - 170$
[7] $t_{cdf} = t_W\ (\Phi L) + t_r - 70$
[8] $t_W\ (MRL) = t_c - 30$
[9] $t_W\ (MRH) = t_W\ (\Phi H) + t_f - 20$
[10] $t_W\ (WR) = t_c - 30$
[11] $t_{mr} = 2t_c + t_W\ (\Phi H) + t_f - 65$
[12] $t_c = t_W\ (\Phi H) + t_W\ (\Phi L) + t_r + t_f$

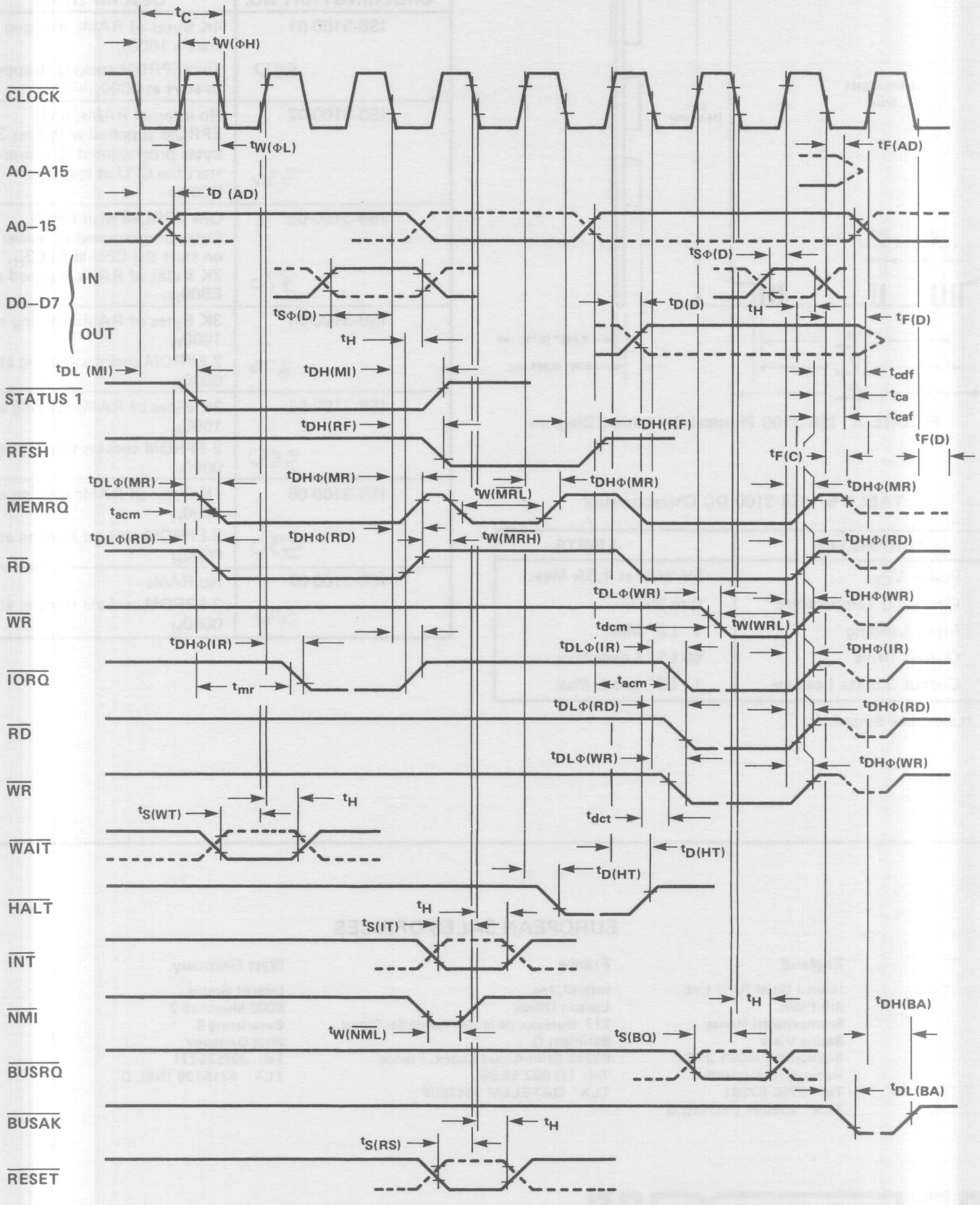

FIGURE 2. ISB-3100 Timing Diagram

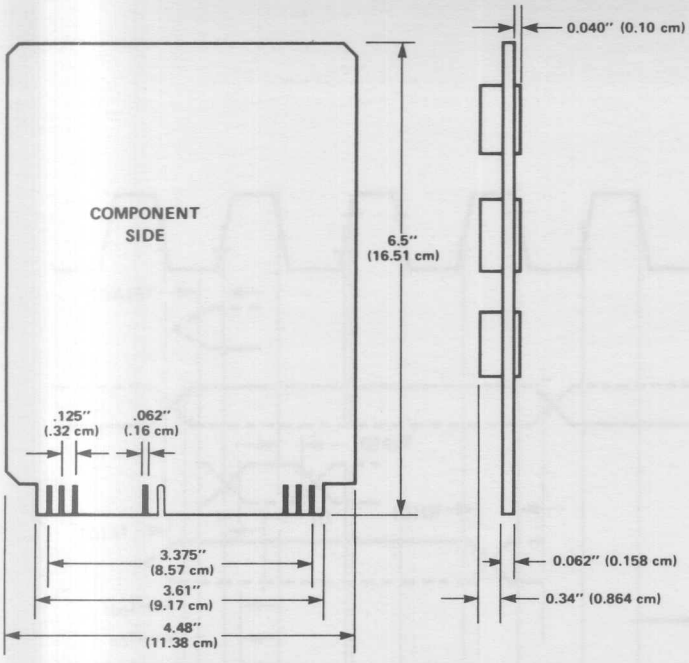

FIGURE 3. ISB-3100 Physical Dimension Diagram

ORDERING INFORMATION

ORDERING PART NO.	DESCRIPTION
ISB-3100-01 390	4K Bytes of RAMs strapped to start a 1000_H Two EPROM sockets strapped to start at 0000_H
ISB-3100-02 330	No internal RAMs, one EPROM supplied with first 3 bytes programmed to power-on start the CPU at location $E000_H$
ISB-3100-03 370	One EPROM with first 3 Bytes programmed to power-on start the CPU at $E000_H$. 2K Bytes of RAMs mapped at $E800_H$.
ISB-3100-04 370	3K Bytes of RAMs starting at 1000_H 2 EPROM sockets starting at 0000_H
ISB-3100-05 350	2K Bytes of RAMs starting at 1000_H 2 EPROM sockets starting at 0000_H
ISB-3100-06 330	1K Bytes of RAMs starting at 1000_H 2 EPROM sockets starting at 0000_H
ISB-3100-07 310	No RAMs 2 EPROM sockets starting at 0000_H

TABLE 5. ISB-3100 DC Characteristics

PARAMETER	LIMITS
Power V_{CC}	5V ±5% at 1.5A Max.
Operating Temperature	0 to 55° C
Input Loading	1 LS* Max.
Output Drive	60 LS* Loads Max.
Output 3-State Leakage	1 LS* Loads Max.

*Low-power Schottky.

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